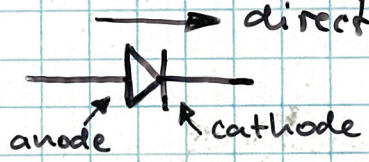
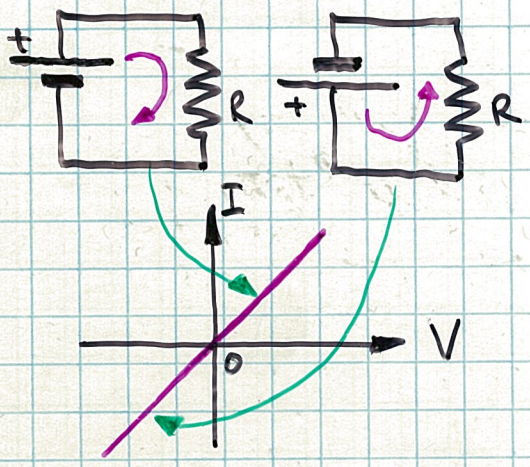
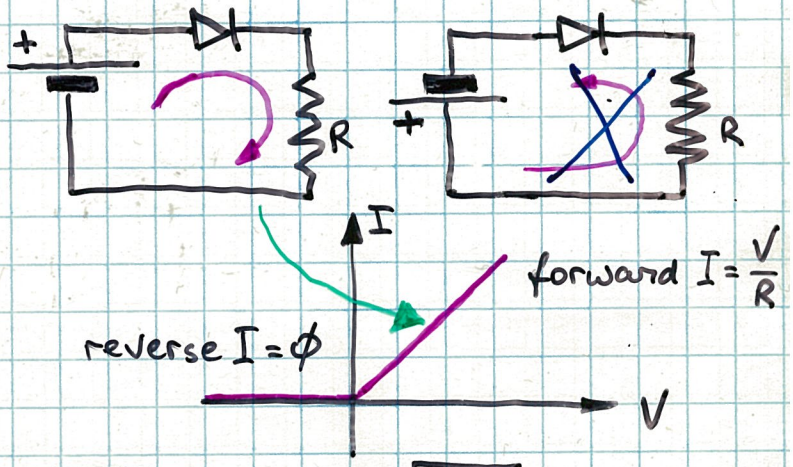
Non-linear circuit elements

DH. Ch.5

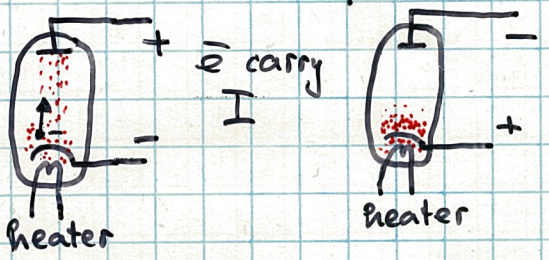
Ideal diodes







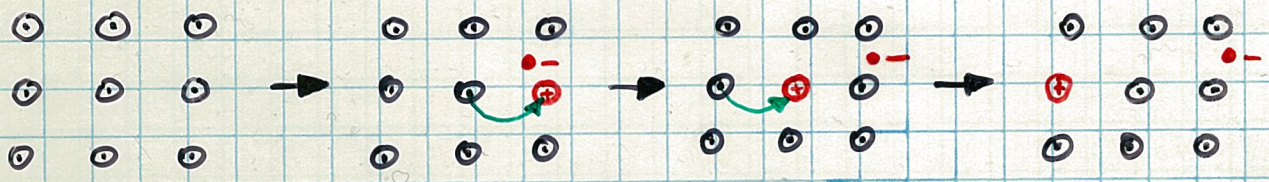
E.g. vacuum diodes



not transpor

Semiconductor diodes

- pure semiconductors (Si, Ge)



electron transport →
hole transport ←
} intrinsic carriers

pure semiconductor: $N_{holes} = N_{\bar{e}} \Rightarrow \frac{1}{2}$ current is carried by $\bar{e}$, $\frac{1}{2}$ by holes.

- recombination is a function of temp. From stat mech: conductivity $\propto$ density of charges $\propto \exp(aT)$!

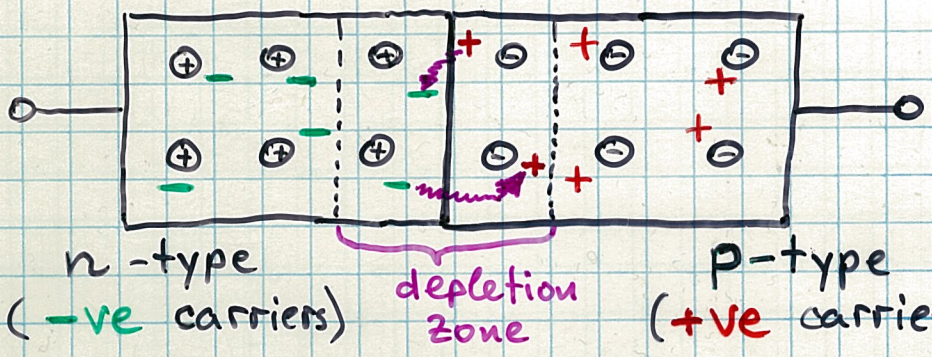
- doped semiconductors : add impurities

impurity = (3+) = hole ⇒ majority carrier is a hole (positive) ⇒ p-type
(e.g. B; acceptor)

impurity = (5+) = $\bar{e}$ ⇒ majority carrier is $\bar{e}$ (-ve) ⇒ n-type
(e.g. P; donor)

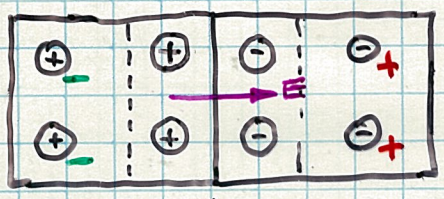
At room temperature, about 1 in 10^{12} atoms in pure semiconductor is thermally excited into an electron-hole pair. In doped semiconductors, extrinsic carriers can have concentration of several ppm → 1,000,000 times higher!
N.B. doping can be controlled.

- pn junction

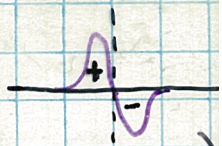


near the contact region, there is a tendency for excess carriers in one region to diffuse into the other region, and to recombine, leaving lower than usual concentration of free carriers near the junction – a depletion zone

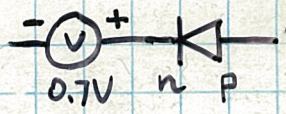
Depletion produces a dipole field across the junction, i.e. a barrier voltage

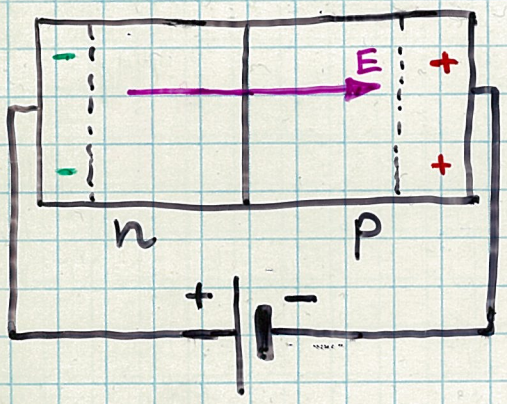


$\Delta V \equiv$ contact potential

E = electric dipole field 

$\Delta V \approx 0.7V$ (Si, room temperature)

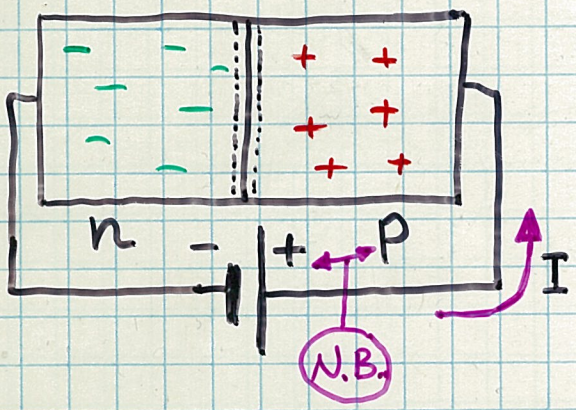
i.e. <u>real</u> Si diode = 



reverse biased

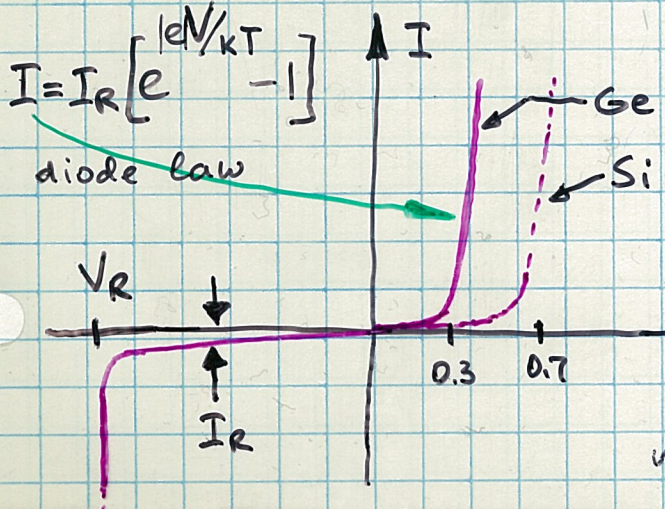
- depletion layer is widened
- no carriers in the depletion region ⇒ no current.

$I \approx 0$ through the junction



forward biased

- external E field overcomes the dipole field & forces the charges into the depletio layer
- no separation of charges, $\Delta V \approx 0$ across the junction.

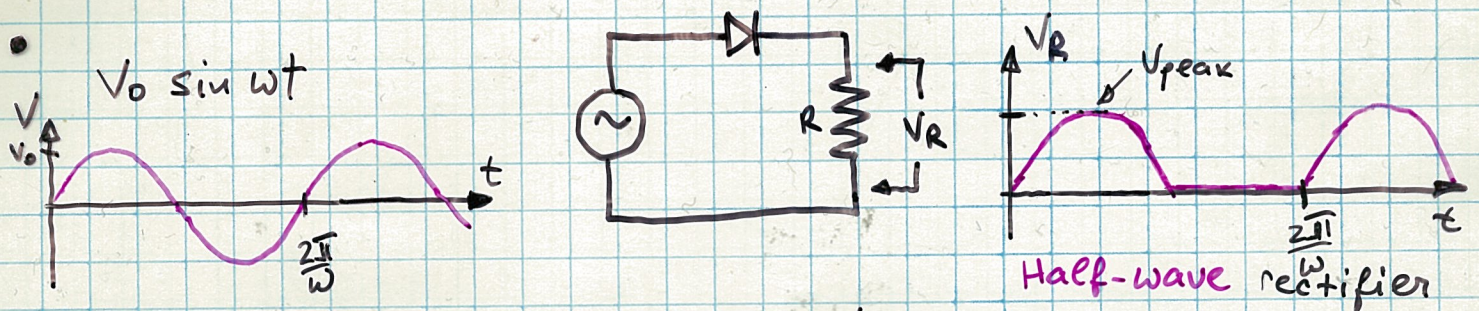


V_R = reverse breakdown voltage

I_R = reverse leakage current, ~ 0.01 μA for Si

minority carriers!

Rectifier circuits (using diodes)

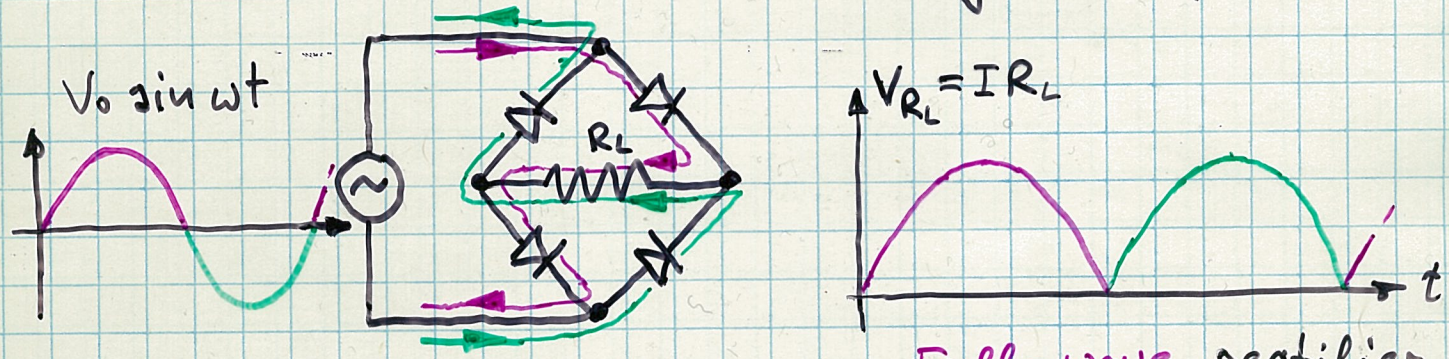


Half-wave rectifier

For a silicone diode, $V_{peak} = V_0 - 0.7V$, and the voltage is present for $\lesssim \frac{1}{2}$ cycle. Ideal diode: $V_{peak} = V_0$

Average (DC) voltage: $\overline{V_{DC}} = \frac{V_0}{T}\int_0^{T/2} \sin \omega t\, dt = \frac{V_0}{\pi}$

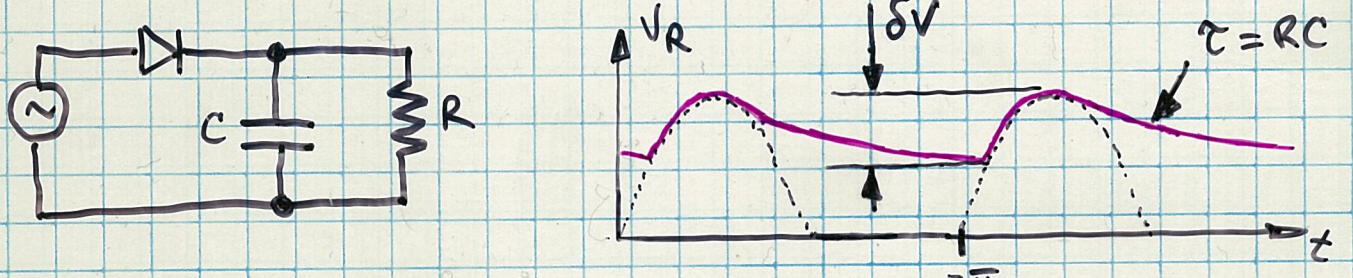
- Half-wave rectification: $\frac{1}{2}$ the time, no current
  Full-wave rectification: can do better by clever switching of the paths!



Full-wave rectifier

Here $\overline{V_{DC}} = \frac{V_0}{T}\int_0^{T} |\sin \omega t|\, dt = \frac{2V_0}{\pi}$

- AC → DC conversion: need a low-pass filter



Real output: DC + "ripple"

$\overline{V_{DC}} + \delta V$

shown for $\omega RC \gg 1$

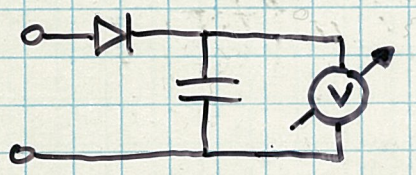
Peak-to-peak ripple voltage is

$$\delta V \simeq V_o\left(1-e^{-T/RC}\right) \simeq \frac{2\pi V_o}{\omega RC}$$

$$\Rightarrow \quad \frac{\delta V}{V_{DC}} \propto \frac{T}{RC} = \frac{T}{\tau}$$

Bridge rectifier (full-wave) reduces this by $\frac{1}{2}$

- AC meters

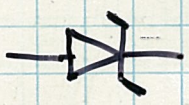


peak-reading AC voltmeter

Sinusoidal input → $V_o = \sqrt{2}\, V_{rms}$

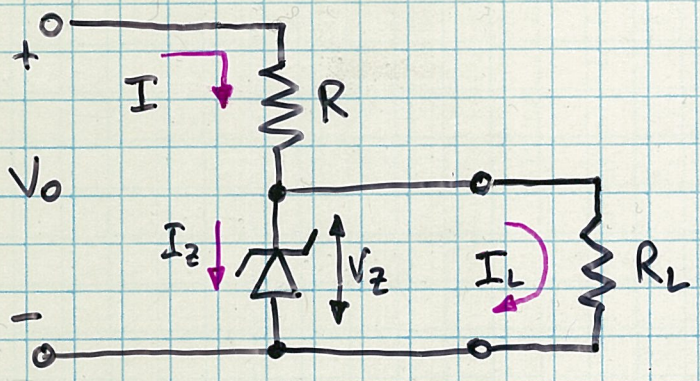
- need corrections for non-ideal diodes
- readings not valid for non-sinusoidal input voltages; use with caution

Voltage references



(using diodes II)

Zener diodes operate in reverse-breakdown mode to take advantage of the well-defined voltage at which it occurs for every given diode.



Voltage across Zener diode = const. (rating)

$$I_L = \frac{V_z}{R_L}$$

$$I = \frac{V_o - V_z}{R}$$

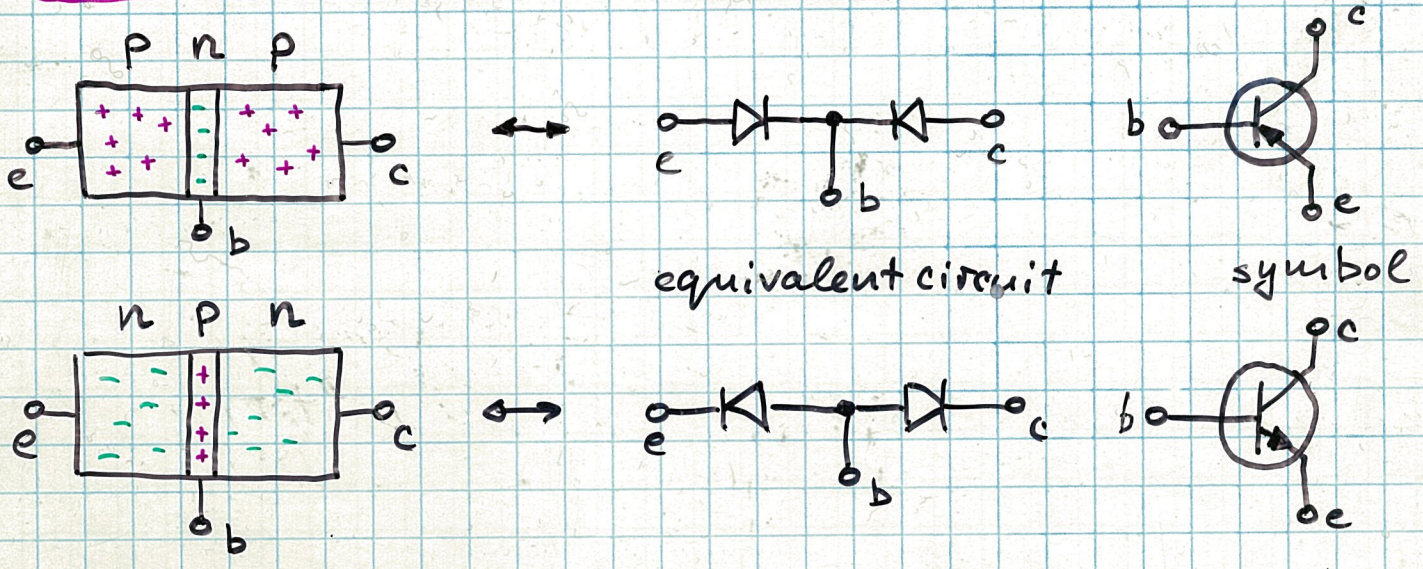
$$I_z = I - I_L$$

as long as $I_z <$ operating limit of diode

NB: in normal operation, the cathode of a Zener diode is +ve.

Transistors: an introduction

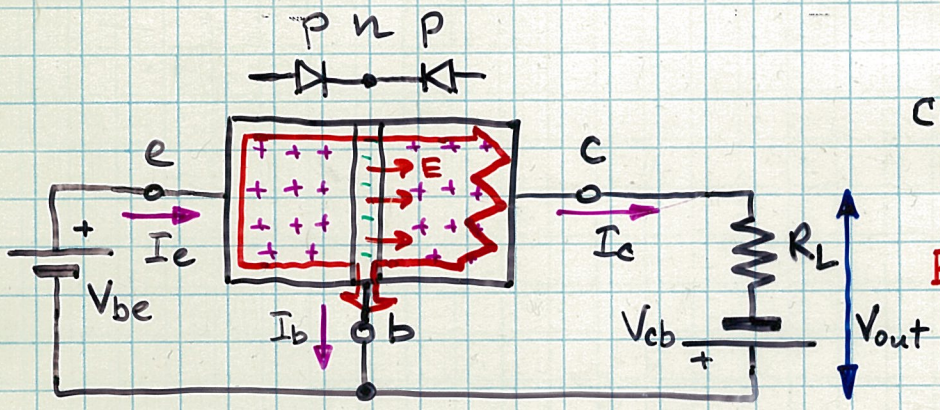
DH Ch. 8



Middle layer: very thin

3 electrodes: base, emitter, collector

Conduction by both e^- and h^+ → bipolar transistors

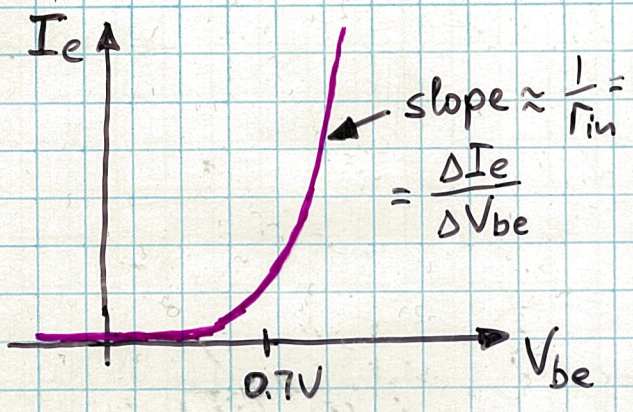


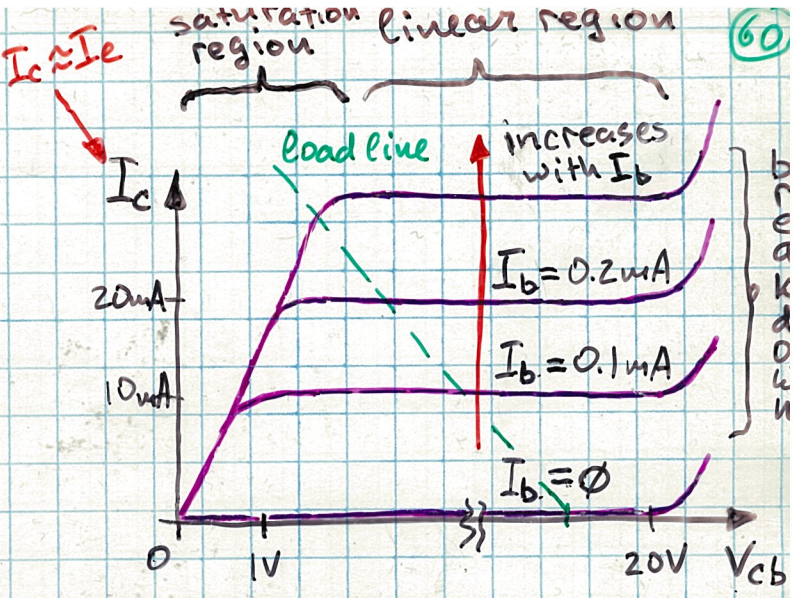
Common base configuration

E = dipole field across cb junction

- eb junction is biased forward ⇒ holes are injected into base region.
- cb junction is reverse biased ⇒ exists a dipole field across cb junction s.t. the holes injected into the base are swept into the collector. Because of the geometry, most holes end up in the collector ⇒ $I_c \lesssim I_e$
- if V_{be} is reversed, the eb junction is reverse biased ⇒ no current flows, since cb junction (also r.b.) does not inject holes into base ⇒ no current

- VI characteristics





r_{in} = input impedance (of the eb junction)
typically, $r_{in} \approx 100\,\Omega$

along the load line:
$V_{out} = V_{cb} - I_c R_L$

- pnp transistor as an amplifier

① KCL: $I_e = I_c + I_b$ with $I_b \ll I_c \lesssim I_e$

② small changes in V_{be} ⇒ VI characteristic is approx. linear: $I_e \approx \frac{V_{be}}{r_{in}}$ [+ const]

③ $V_{out} = V_{cb} - I_c R_L \approx V_{cb} - I_e R_L = V_{cb} - \frac{V_{be}}{r_{in}} R_L$

⇒ $\Delta V_{out} = \frac{\Delta V_{be}}{r_{in}} R_L$

⇒ Voltage gain $= G_v \equiv \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{\Delta V_{out}}{\Delta V_{be}} = \frac{R_L}{r_{in}}$

typically, $r_{in} \approx 100\,\Omega$, $R_L \approx 10\,k\Omega$ ⇒ $\boxed{G \approx 100}$

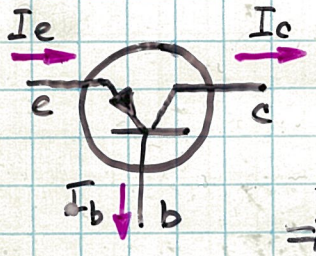
⇒ small changes in the V_{be} cause large changes in V_{out} ⇒ amplifier

- saturation: rapid buildup of I_c as excess h^+ are allowed to pass into c.
linear ("active"): all excess h^+ go into c.

- current gain

α = fraction of h^+ diffusing across narrow b region

$1-\alpha$ = fraction of h^+ recombining with e^- in b

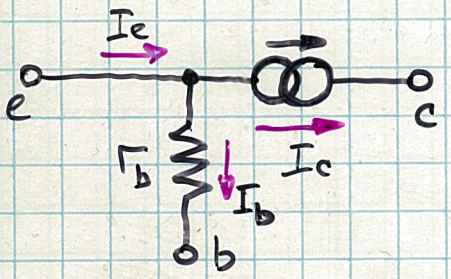


$$\left.\begin{aligned} I_c &= \alpha I_e \\ I_b &= (1-\alpha) I_e \end{aligned}\right\} \quad \begin{aligned} G_i &= \frac{I_c}{I_e} = \alpha \\ \beta &\equiv \frac{I_c}{I_b} = \frac{\alpha}{1-\alpha} \end{aligned}$$

$\Rightarrow$ G_i fairly constant over active region

- once the operating point has been established, i.e. once different bias voltages have been chosen (thus fixing r_{in}, for example), variations due to small signals can be treated as approx. linear:

Reduced T model

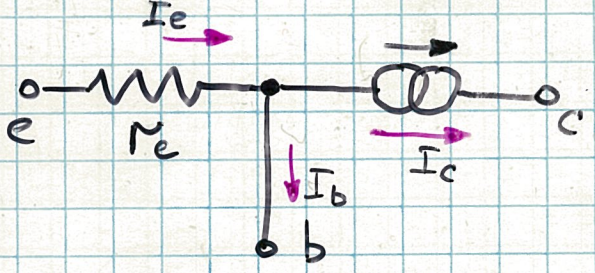


$$I_c = \alpha I_e = \beta I_b$$

$$G_v = \frac{V_{out}}{V_{in}} = \frac{I_c R_L}{I_b r_b} = \frac{\beta R_L}{r_b} = \frac{R_L}{r_{in}}$$

$$\Rightarrow \quad r_{in} = r_b/\beta$$

Ebers-Moll model



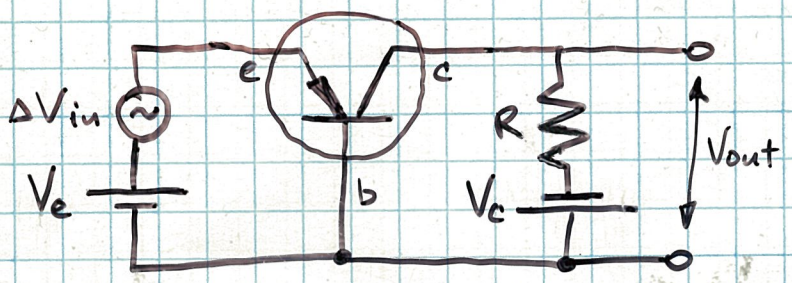
$$I_c = I_e \left[e^{-V_{be}/V_T} - 1 \right]$$

$$V_T = \frac{kT}{q_e} \simeq 25 \text{ mV} \text{ @ } 20^\circ\text{C}$$

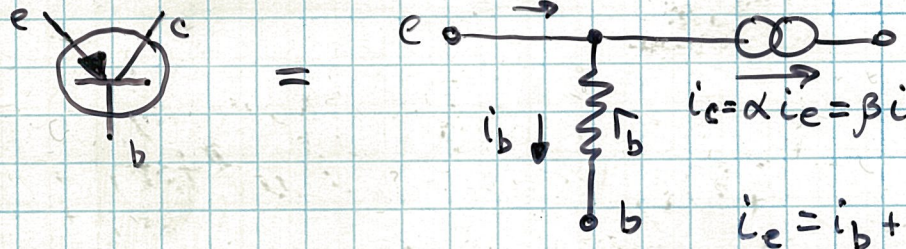
$$r_{in} = r_e = \frac{V_T}{I_c} = \frac{25 \cdot 10^{-3}}{I_c} \ \Omega$$

- model's parameters vary when the operating point is changed; need to look them up in data tables.

Ex. Common-base amplifier



typical values
$R = 10{,}000\,\Omega$
$r_b = 800\,\Omega$
$\beta = 100$

$\Rightarrow$ 

with i_e, i_b, i_c indicating the small signal currents

$\Rightarrow \Delta V_{in} = i_b r_b$

$\Delta V_{out} = i_c R = \alpha i_e R = \beta i_b R$

$\beta = \frac{\alpha}{1-\alpha} \Leftrightarrow \alpha = \frac{\beta}{1+\beta}$

$$\Rightarrow G_v = \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{\beta i_b R}{i_b r_b} = \beta \frac{R}{r_b} = \frac{1}{8} \cdot 10^4 = 1250$$

$$G_i = \frac{i_{out}}{i_{in}} = \frac{i_c}{i_e} = \alpha = \frac{\beta}{1+\beta} \approx 0.99$$

Power gain $G_p = G_v G_i \approx 1238$

$r_{in} = \frac{r_b}{\beta} = 8\,\Omega$ — low

$r_{out} = R = 10{,}000\,\Omega$ — high

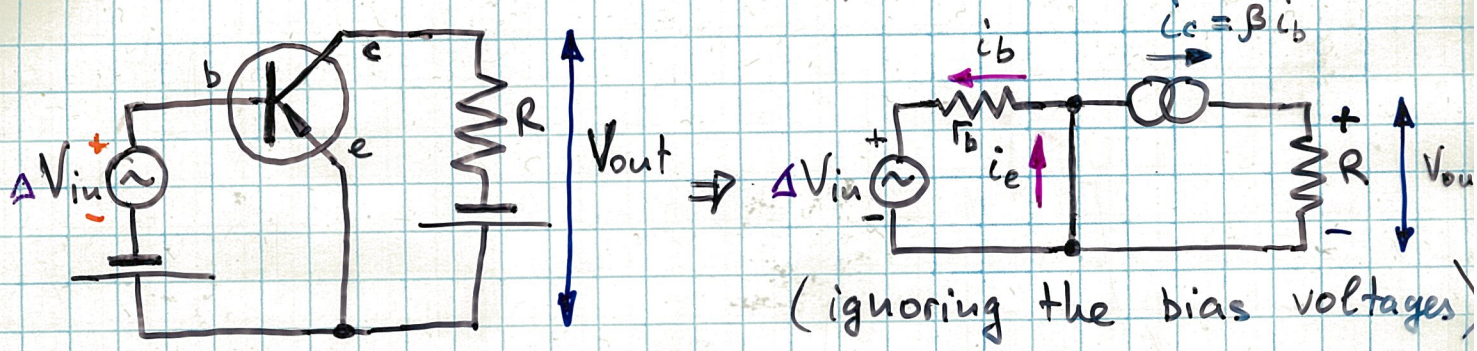
} impedance transformer 8 : 10,000

Note: $G > 0 \Rightarrow$ non-inverting amplifier

The same transistor can be connected in a different manner, e.g. common-emitter configuration. The analysis of this circuit is similar to the common-base configuration.

In brief:

Ex. Common-emitter amplifier



(ignoring the bias voltages)

! Keeping the signs straight !

- since the emitter-base junction is biased forward, a small +ve ΔV_{in} will decrease the base current, i.e. cause a −ve i_b

- $\Delta V_{in} = -i_b r_b$
  $\Delta V_{out} = i_c R = \beta i_b R$
  $\Big\} \Rightarrow G_v = \dfrac{\beta R}{-r_b} = -\beta \dfrac{R}{r_b}$

For the same values as before:

$\beta = 100 \quad r_b = 100\,\Omega \quad R = 10{,}000\,\Omega \Rightarrow G_v = -1250$

(inverting amp!)

- $G_i = \dfrac{i_c}{i_b} = \beta = 100$ (was 0.99)

- $|G_p| = |G_v G_i| = 125{,}000$ (was 1238)

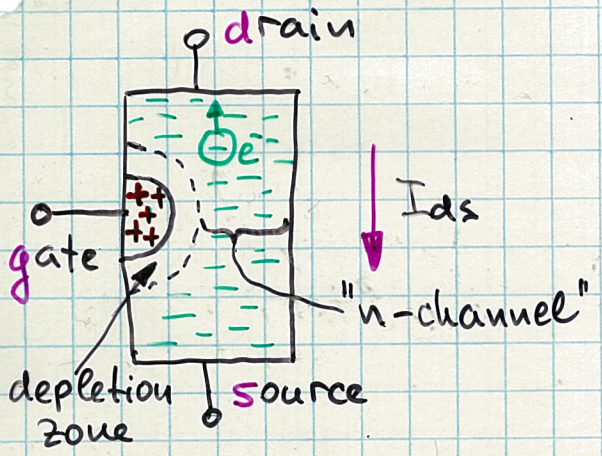
- $r_{in} = r_b = 800\,\Omega$
  $r_{out} = R = 10{,}000\,\Omega$
  $\Big\}$ impedance ratio now 8 : 100 (was 8 : 10,000)

Common-base: modifies impedance, $G_i \approx 1$

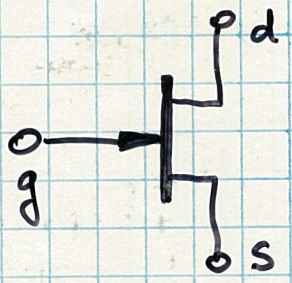
Common-emitter: high G_v and high G_i

JFETs

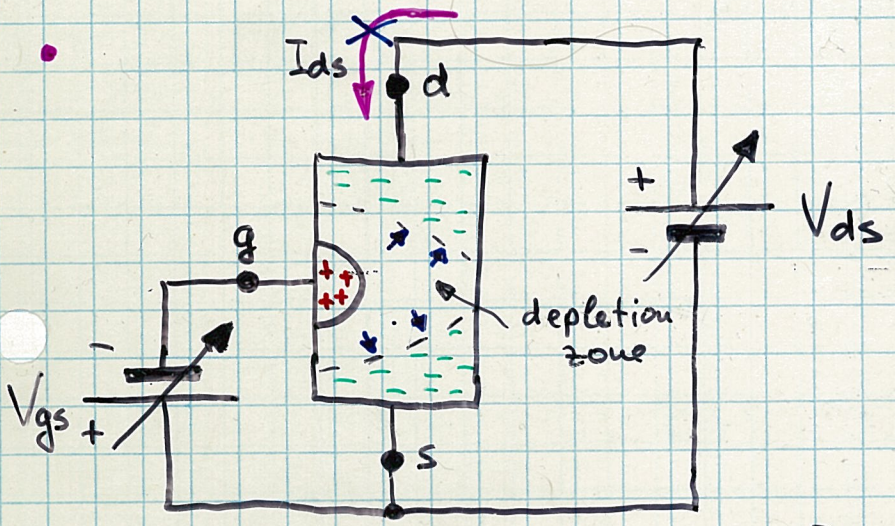
- n-channel Junction Field-Effect Transistor



literally: source and drain of e⁻



← in practice, d & s are sometimes interchangeable.

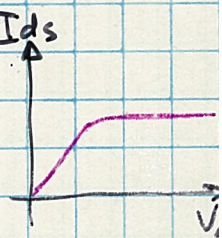
- 

① When $V_{gs} = 0$ ("grounded gate")
I_{ds} flows easily (ON, $R \sim 25$–$100\,\Omega$), limited by the max device dissipation rating, $I_{ds} V_{ds}$

② Increase V_{gs} as shown ⇒ gate-channel diode is highly reverse-biased ⇒ depletion zone widens all the way across the n-channel ⇒ current I_{ds} is completely "pinched off" (OFF, $R \sim 10^9\,\Omega$)

Typical $V_{gs,OFF} \sim -2$ to -15 V (JFETs used as switch

- I_{ds} dependence on V_{ds}
  - V_{ds} small: $I_{ds} \propto V_{ds}$ (Ohmic region)
  - V_{ds} large: I_{ds} saturates (pinch-off region)

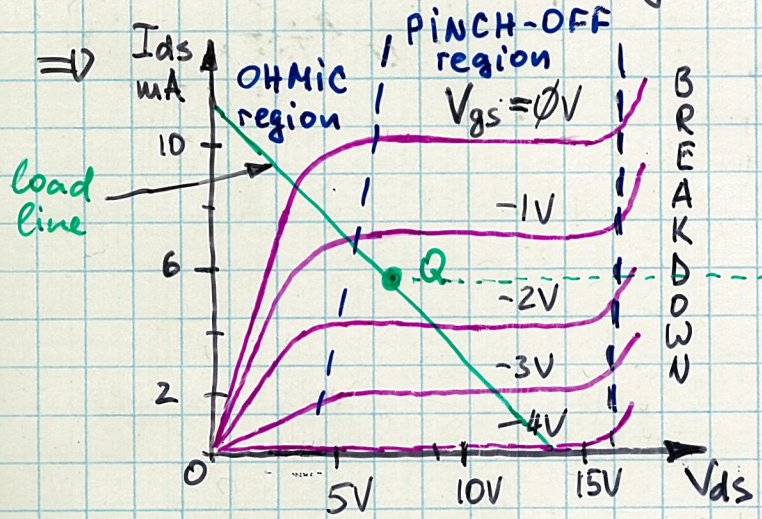


Reason: ohmic (IR) voltage drop across the channel increases with I_{ds} and pushes the gate potential (already -ve relative to s) even more -ve relative to d ⇒ increasing reverse bias ⇒ pinching I_{ds} more

! Negative feedback: two effects cancel ⇒ saturation.

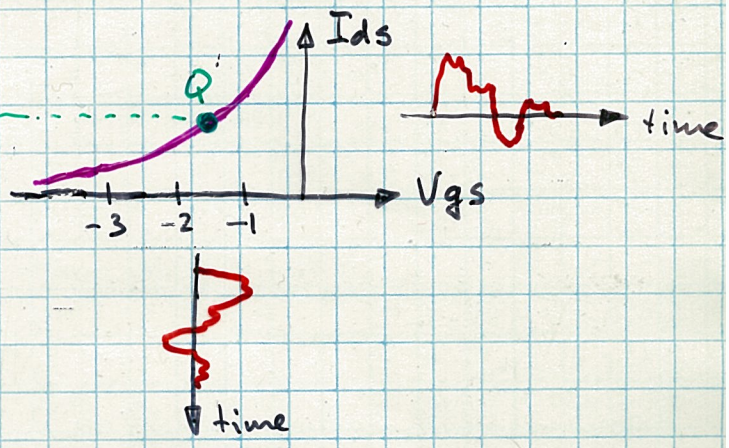
- I_{ds} still depends on V_{gs}, of course.

⇒



Here $V_{gs,OFF} \simeq -4V$

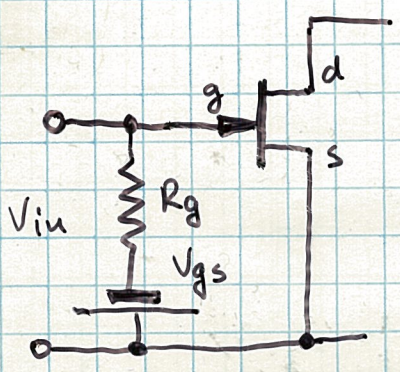
Changes in V_{gs} cause changes in I_{ds}



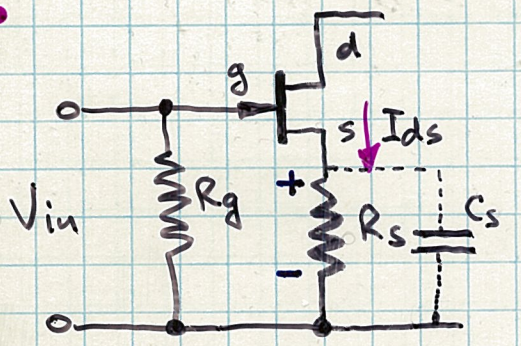
V_{gs} (and I_{ds}) have a dc component which is the average value of the input voltage (output current) ⇒ we are working in the regime of small signals (AC) about those time-average values (DC).

These average (DC) values are known as quiescent voltage and current, or a quiescent operating point Q, about which the signal varies

Notes on practical JFET circuits

- 

Gate-source leakage current is small (the resistance of a reverse-biased g-s junction is high) ⇒ to control input impedance, add $R_g \lesssim 1\text{-}10\,M\Omega$

- 

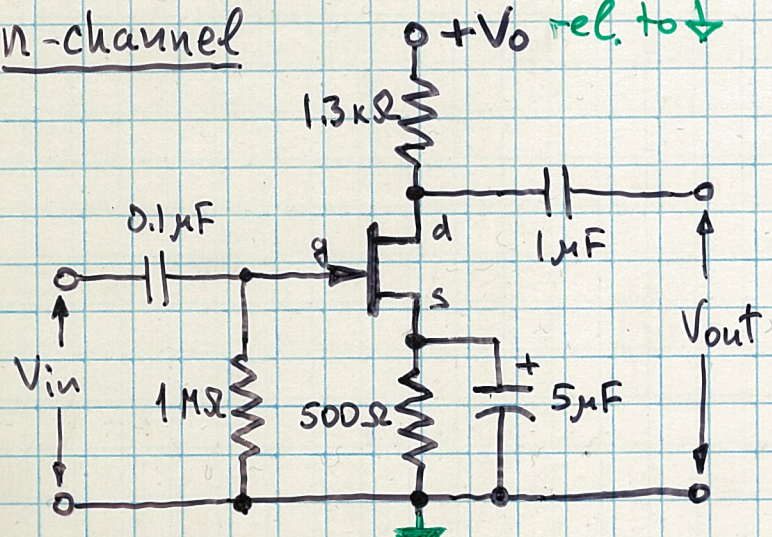
Inconvenient to need a second battery to supply V_{gs}. Use self-biasing by including a series $R_s \sim 1\,k\Omega$. Voltage drop across R_s is $I_{ds}R_s$, -ve bias of g relative to s

Also: can use a C_s in parallel to R_s to smooth out AC variations due to input signals.

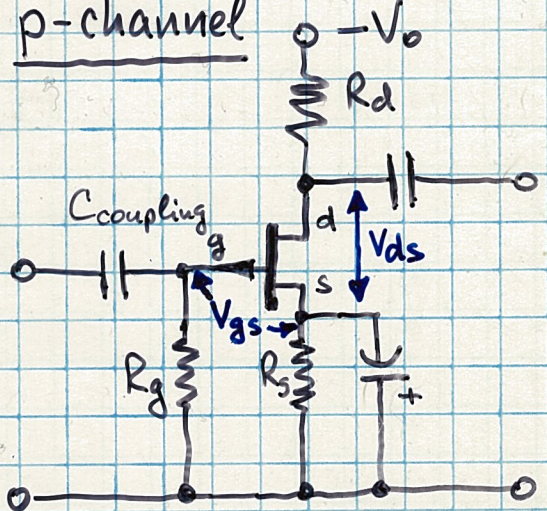
- Add capacitors in series at the input and output: DC currents will be "confined" to the FET circuit, and the AC [small] signals will flow freely across C's

Ex1. practical circuits

n-channel



p-channel



Ex2. Lab experiment #5