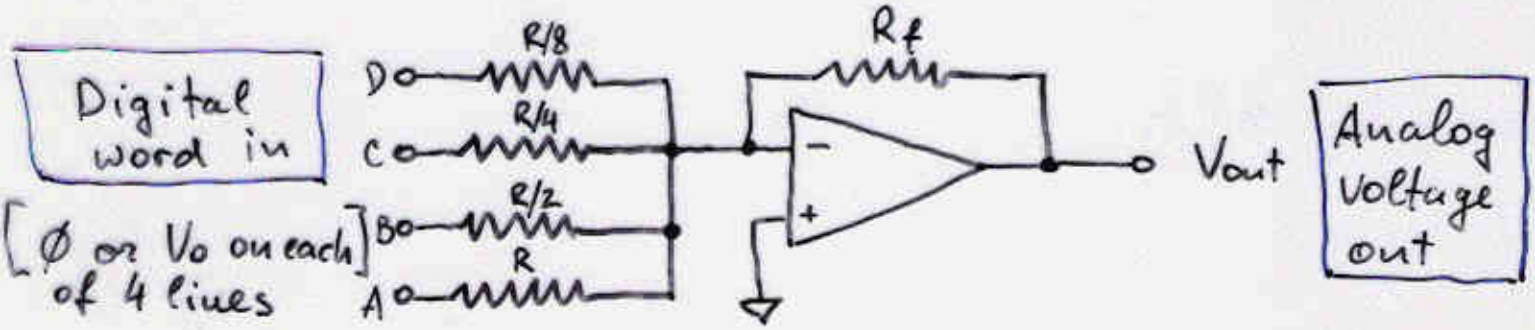
A/D and D/A conversion

D/A converter



weighted-resistor ladder network

$$V_{out} = -V_0 \frac{R_f}{R}\left[A\cdot 1 + B\cdot 2 + C\cdot 4 + D\cdot 8\right]$$

BCD coding!

$(DCBA)_{10}$	DCBA	Vout
Ø	0000	−0.0V
1	0001	−0.5V
2	0010	−1.0V
3	0011	−1.5V
.....	.....	.....
8	1000	−4.0V
9	1001	−4.5V

@ $R_f = R/8$
$V_0 = +4.ØV$

Notes:

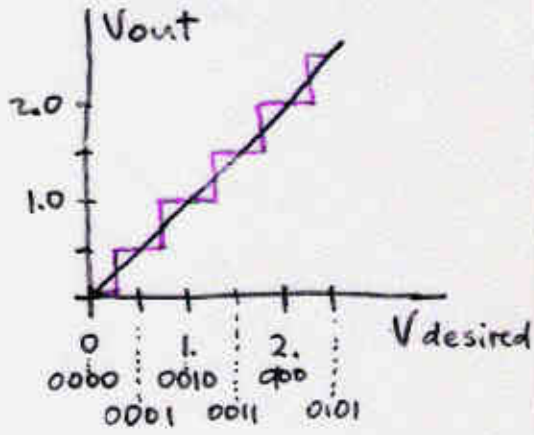
- adjust R_f to avoid saturation
- need good precision resistors
- resolution of an n-bit converter $\approx \frac{1}{2^n}$

E.g. here $\frac{1}{2^4} = \frac{1}{16} = 6.25\%$ i.e. $\pm 3.125\%$ is the inherent uncertainty of the digital representation
→ R_f should be at least as good, so that the scale of output reflects the accuracy of input

- ladder resistors should be good enough to distinguish adjacent voltage values. E.g. for bit D: value = "8", i.e. "$7\frac{1}{2}$" < R_D < "$8\frac{1}{2}$"

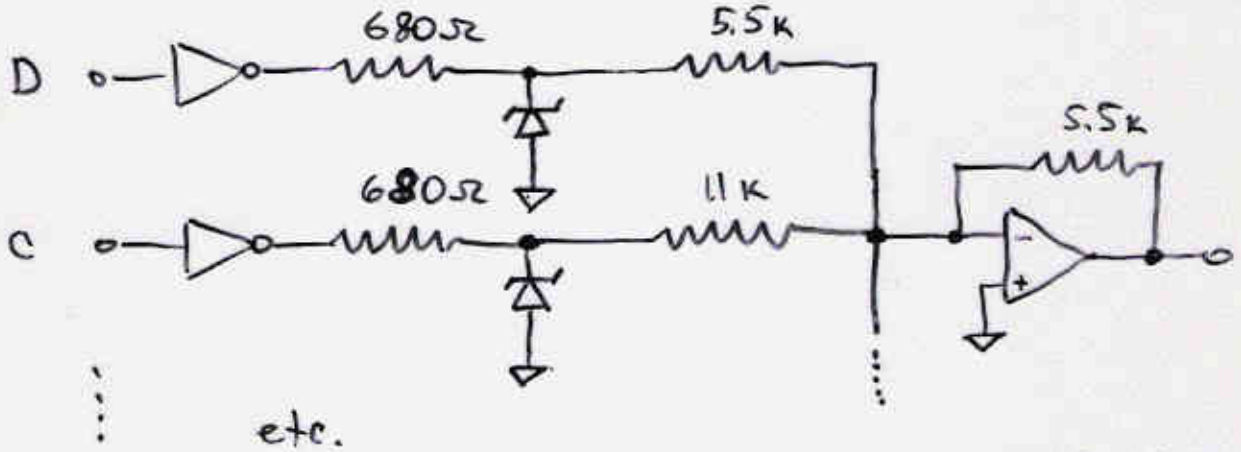
  EFTS: is the tolerance for R_A higher or lower?

- the output of DAC varies in steps, not continuously: To reduce the size of steps need to use a higher # of bits.



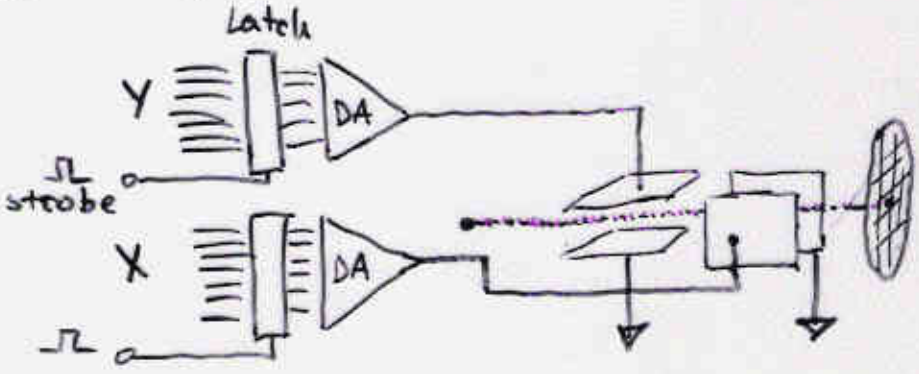
- need good reference V_0 to have reproducible Vout, not usually available in digital circuits!

  ⇒ use diodes for precise level control:

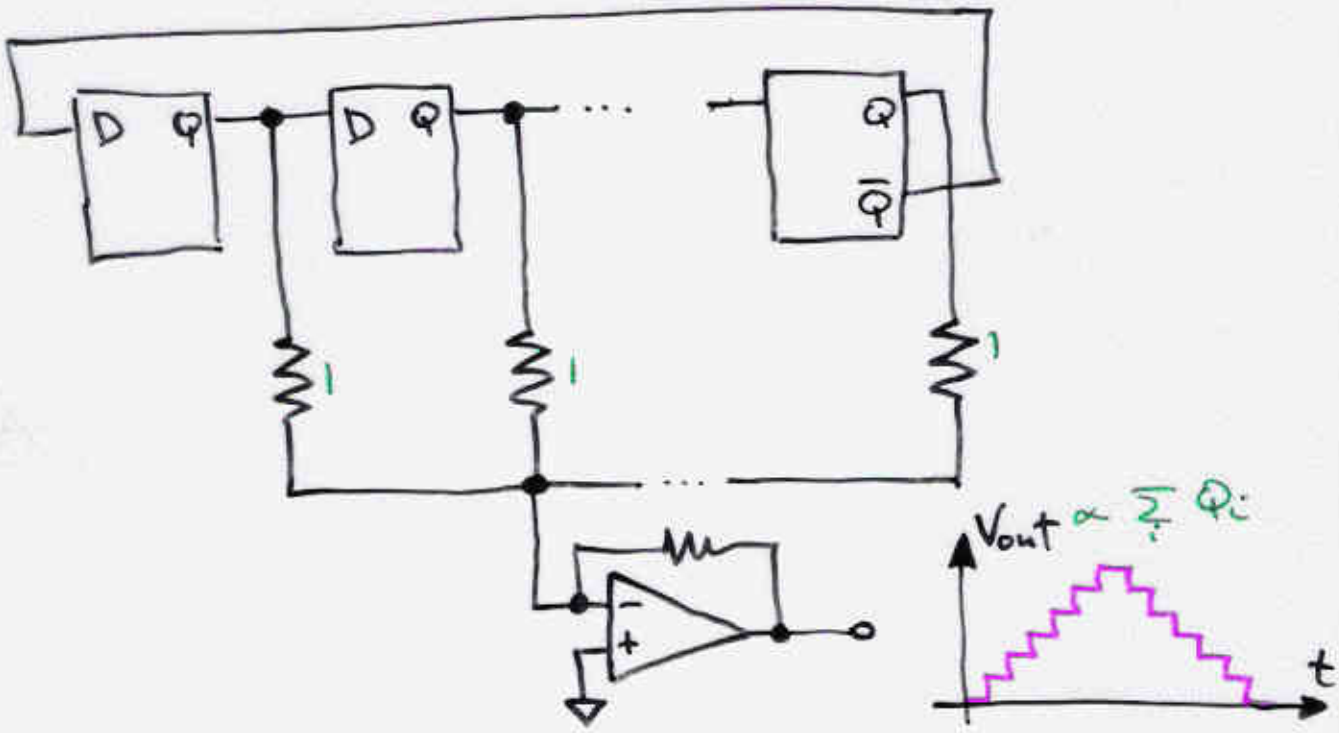


In this typical design, the voltage level of each logic bit is ≈0.7V rather than 3.5 ÷ 5.0 V.

- use to control XY-displays (plotter, CRT)

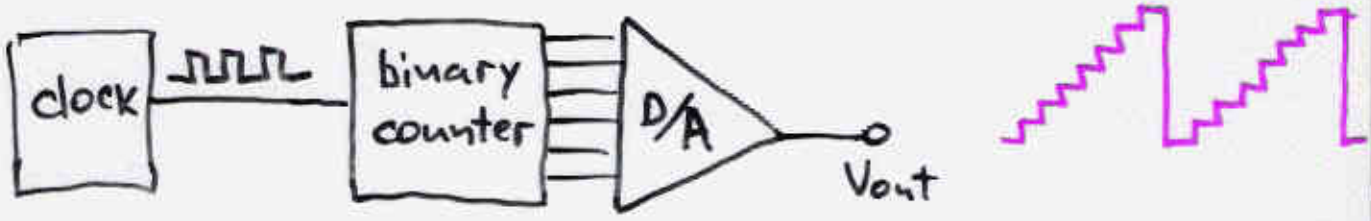


Ex Johnson counter, revisited

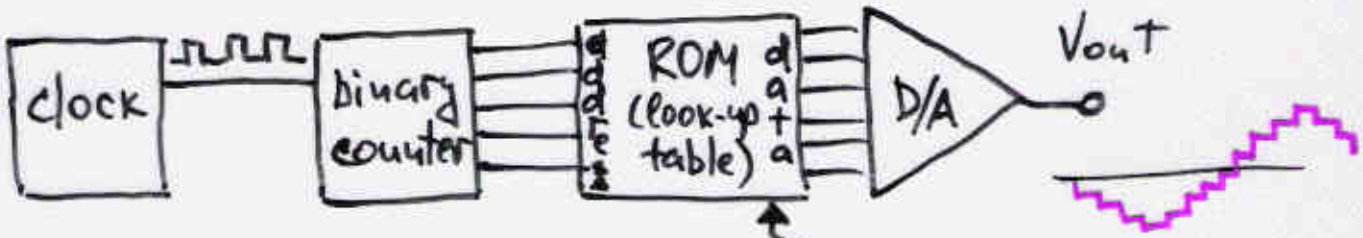


⇒ a triangular analog wave generator

Ex saw-tooth waveform generator

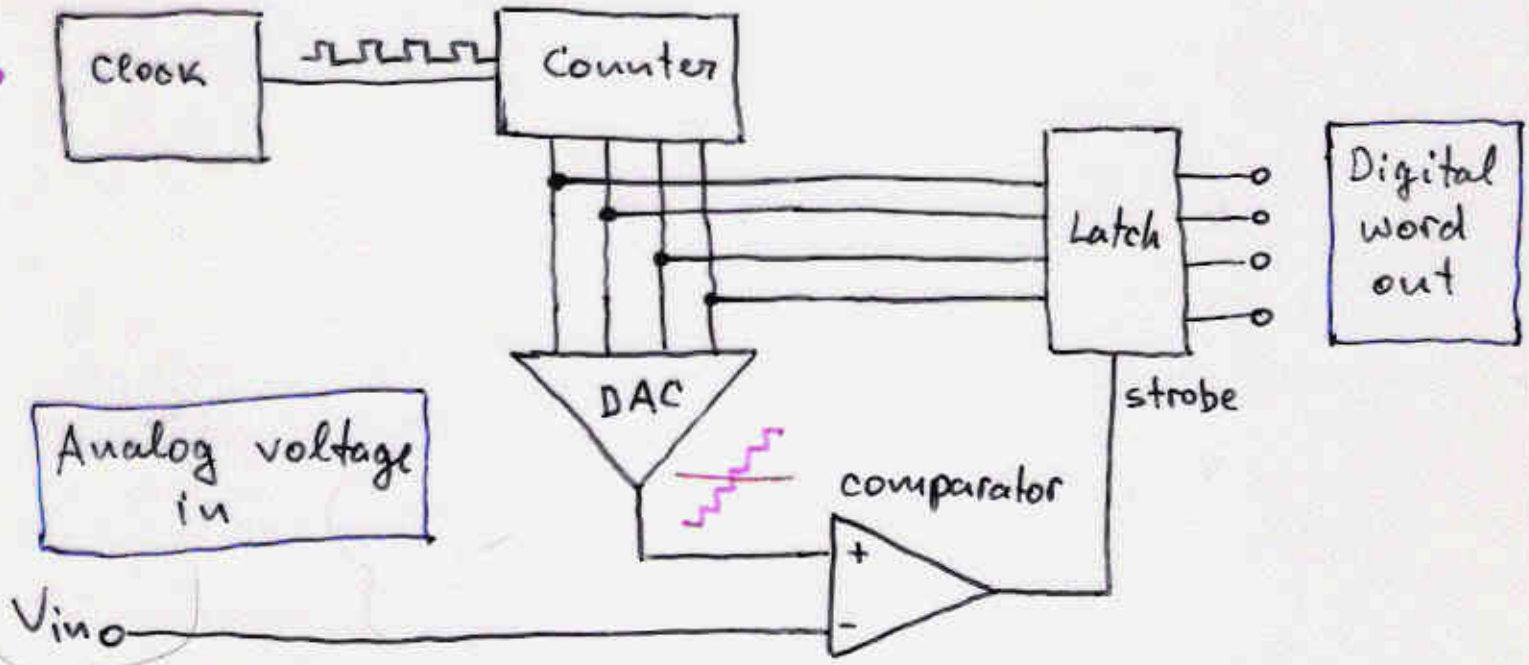


Ex arbitrary waveform generator

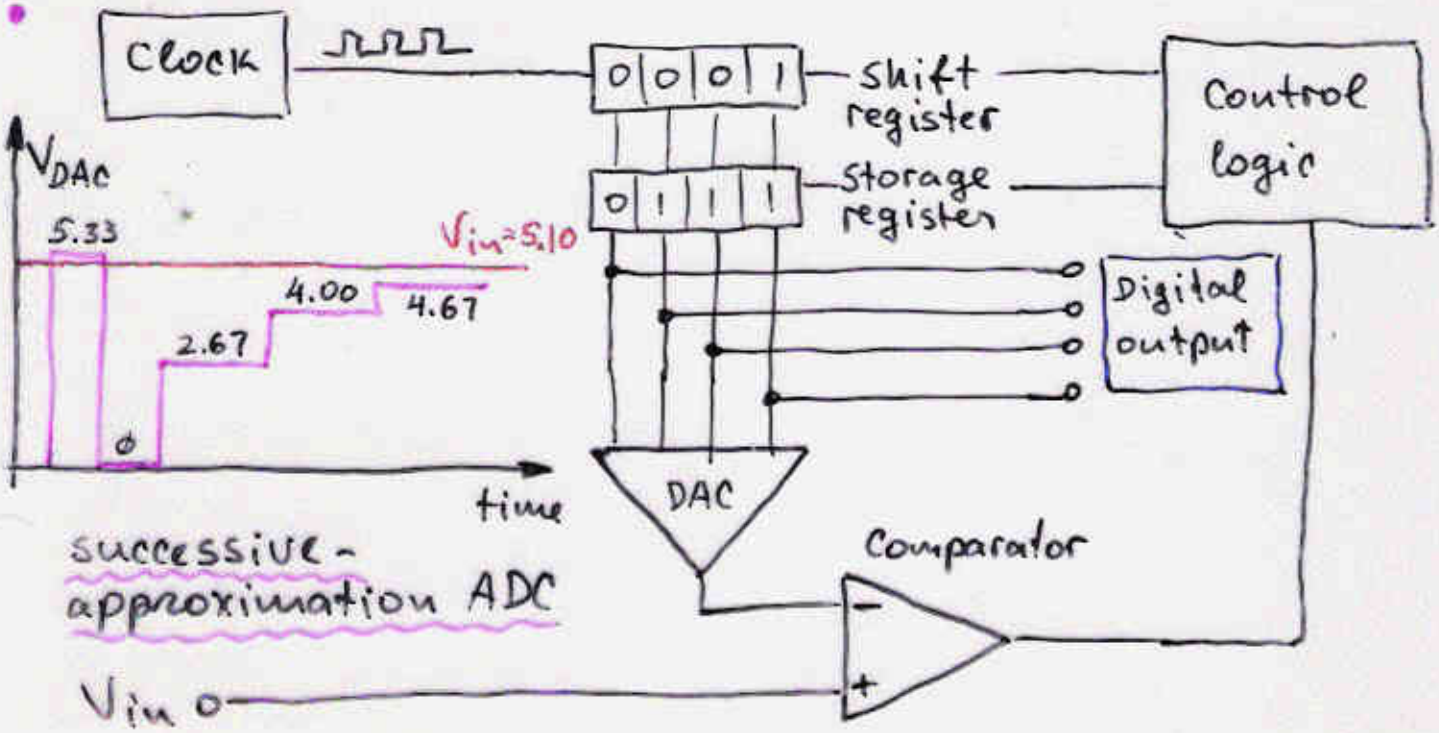


e.g. a sine-wave look-up

A/D converters



- this is "tracking ADC": count until $V_{in} = V_{DAC}$
- slow for high-resolution DACs (large # of small steps)
- can improve by counting up and down, depending on the output of the comparator.

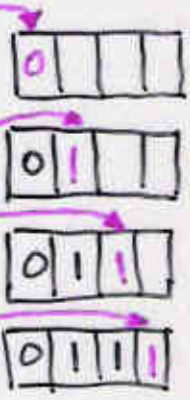


4-bit successive approximation A/D on Ø-10V range.

0000	0001	0010	0100	1000	1111
ØV	0.67V	1.33V	2.67V	5.33V	10V

- perform a series of comparisons between the analog $V_{in} = 5.1ØV$ and a series of reference voltages. If reference = $V_{DAC} \leq V_{in}$, an appropriate bit is set to "1".

1. try 1000 = 5.33V. Too large ⇒ MSB = "Ø"
2. try 0100 = 2.67V. Too small ⇒ 2nd MSB = "1"
3. try 0110 = 4.00V. Too small ⇒ 3rd MSB = "1"
4. try 0111 = 4.67V. Too small ⇒ 4th MSB = "1"

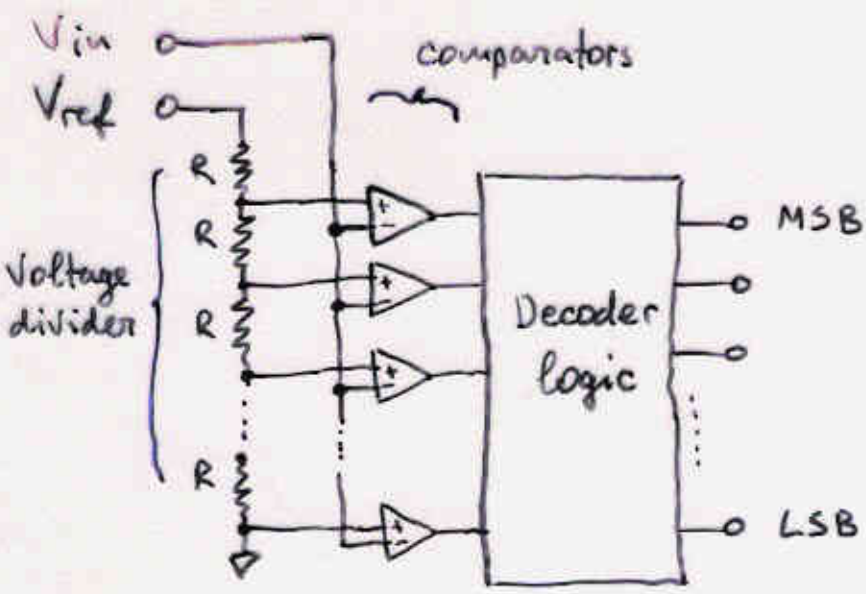


5. report "0111" (= 4.67V) as the digital representation of $V_{in} = 5.10$ V, i.e. "5.10V ≈ 4.67V"

- precision: 1 part in 2^4 or 625 mV in 10V
  i.e. the smallest step = 625 mV.

  ⇒ 5.10 = "somewhere between 4.67 and 5.33"
- resolution: ½ smallest step = 312 mV, i.e. two analog values 312 mV apart will be distinguished, but their absolute values known to within 625 mV

- ADC levels are "quantized" ⇒ quantization noise, or "waffling" of the digital output between two adjacent levels which bracket the true value
- max error when input is ½ way between levels



EFTS
Design the Decoder logic for a 2-bit flash ADC

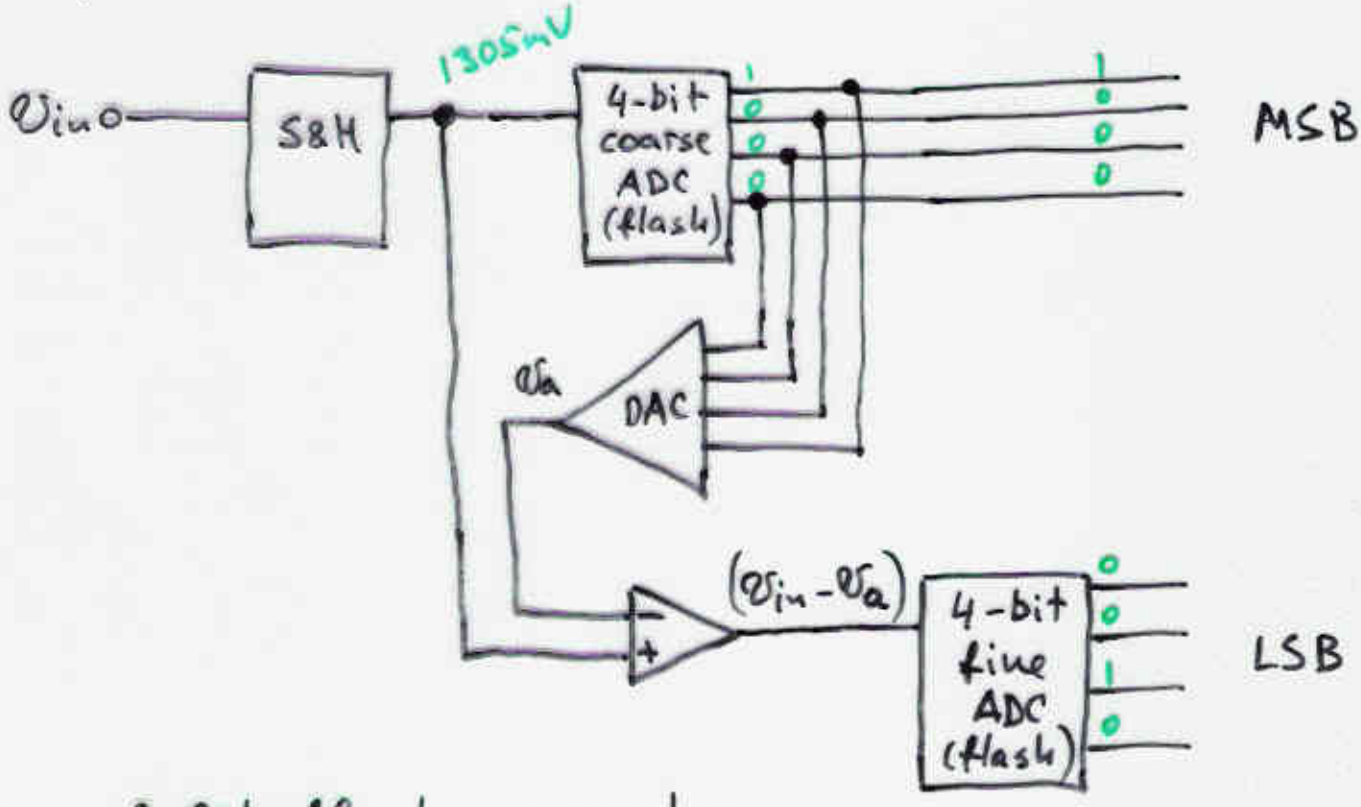
- this is the "flash converter" : all bits are processed in parallel. Conversion time only limited by the propagation delays in the logic, but circuitry more complex

- comparison

tracking	succ. approx.	flash
- cheap, simple - slow-varying signals only - worst-case: $2^n - 1$ steps	- moderate $ $30-100 for 8-12 bit - wide range of sampling rates - conversion in n steps	- complex, $$ - capable of very fast conversions, in 1 step.

- only unipolar, BCD used above. Other coding schemes and bipolar possible E.g. 2's complement, and  for a flash ADC

- parallel-series ADC



One 8-bit flash converter
- 255 comparators in a ladder

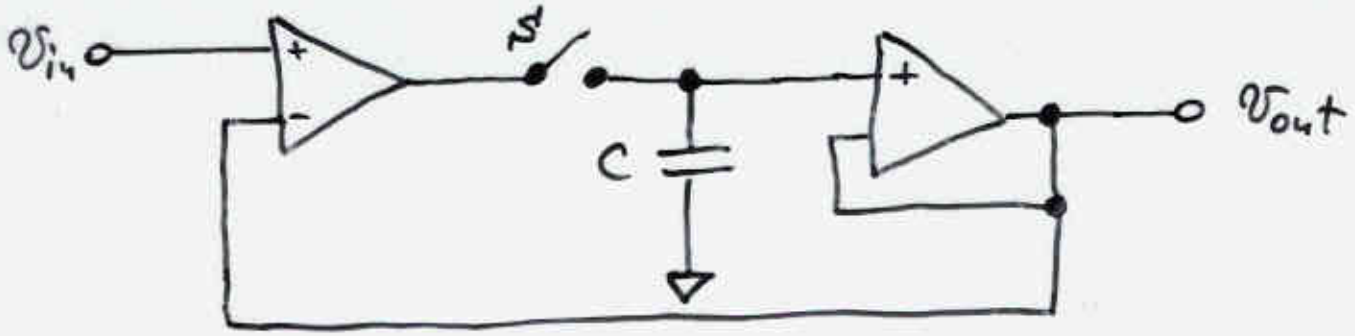
Two 4-bit flash converters
- 2 × 15 = 30 comparators

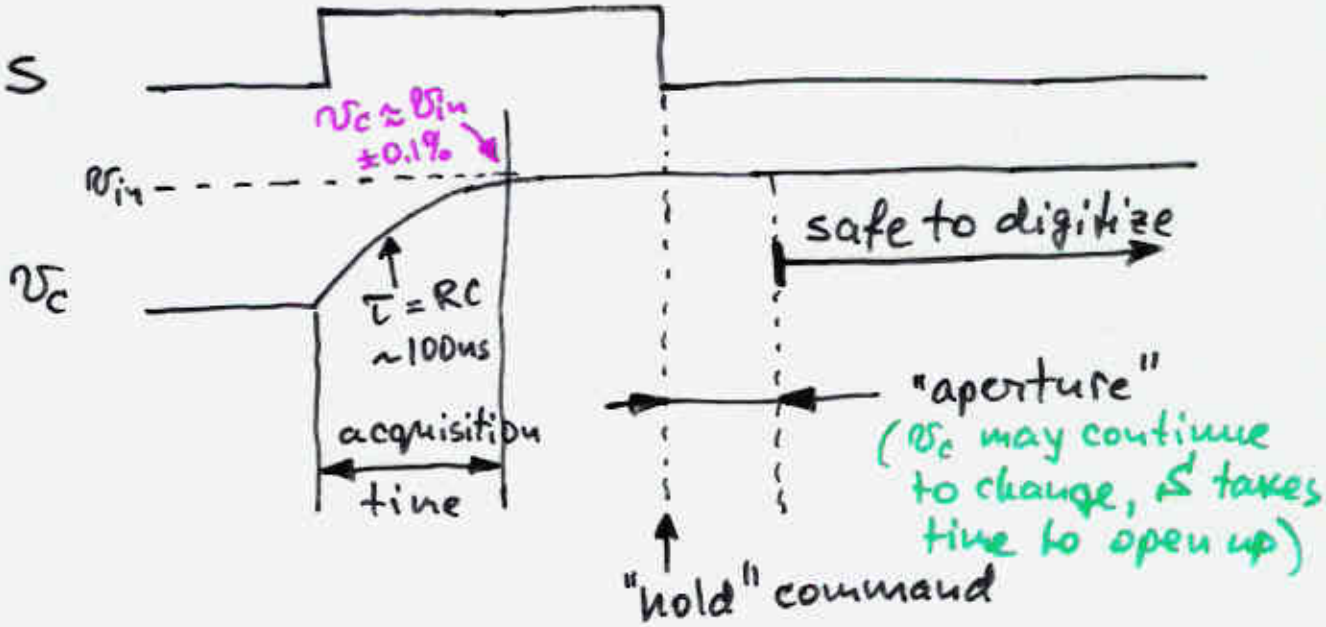
The down side :
- extra components : DAC, fast analog subtractor, S&H

Ex LSB = 10mV, V_{in} = 1305 mV

$2550 \leq V_{in}$	1111	1111
$2540 \leq V_{in} < 2550$	1111	1110
$2530 \leq V_{in} < 2540$	1111	1101
.....		
$1290 \leq V_{in} < 1300$	1000	0001
$1280 \leq V_{in} < 1270$	1000	0000 ← midpoint
.....		
$10 \leq V_{in} < 20$	0000	0001
$0 \leq V_{in} < 10$	0000	0000

- sample-and-hold amplifier





- A/D parameters
  - quantization (digital) error : $\pm \frac{1}{2}$ LSB typ.
  - accuracy : ±1 LSB typ, or % of full scale
  - linearity

$\pm \frac{1}{2}$ LSB is the best possible, ±1 LSB typ

[a common cause of non-linearity is a missing output code, spikes — i.e. non-monotonicity as well as non-linearity]

- Resolution : 2^N levels, $2^N - 1$ steps

$$\frac{1}{2^N - 1} \simeq \frac{1}{2^N}$$

No. bits	No. steps $= 2^N - 1$	LSB, % full scale	Dyn. range, dB
8	255	0.39	48
10	1023	0.098	60
12	4095	0.024	72
14	16383	0.0061	84
16	65535	0.0015	96

ref Simpson p. 744

- Dynamic range : $\frac{V_{largest}}{V_{smallest}}$, usually in dB

$$D.R. = 20 \log \frac{2^N - 1}{1} \simeq 20 \log 2^N$$

- conversion time
- throughput
- S/H droop

Ex I/O board for interfacing a computer to an experiment