

Experiment 2

Logic Gates

The principles of digital logic govern the operation of all modern computers. The objective of this experiment is to become familiar with basic logic gates and their appropriate logic truth tables. These logic gates are then used to construct various simple logic circuits such as an adder, a latch, and a binary counter.

2.1 Circuit assembly techniques

You will be using a breadboard to assemble and test your hands-on circuits. The breadboard provides a convenient and organized way of implementing circuits, making quick component changes and providing trouble-free circuit connections. On the board you have access to five pairs of binding posts BP1-BP5, red and black. Also, there are five BNC coaxial connectors. A cable supplies the board with ± 15 , +5 and 0 Volts DC. The black binding posts and the outer ring of the BNC connectors have a common connection to ground, or 0V. These signals are all available to the protoboard, the matrix that you will build your circuits on, as shown in Figure 2.1.

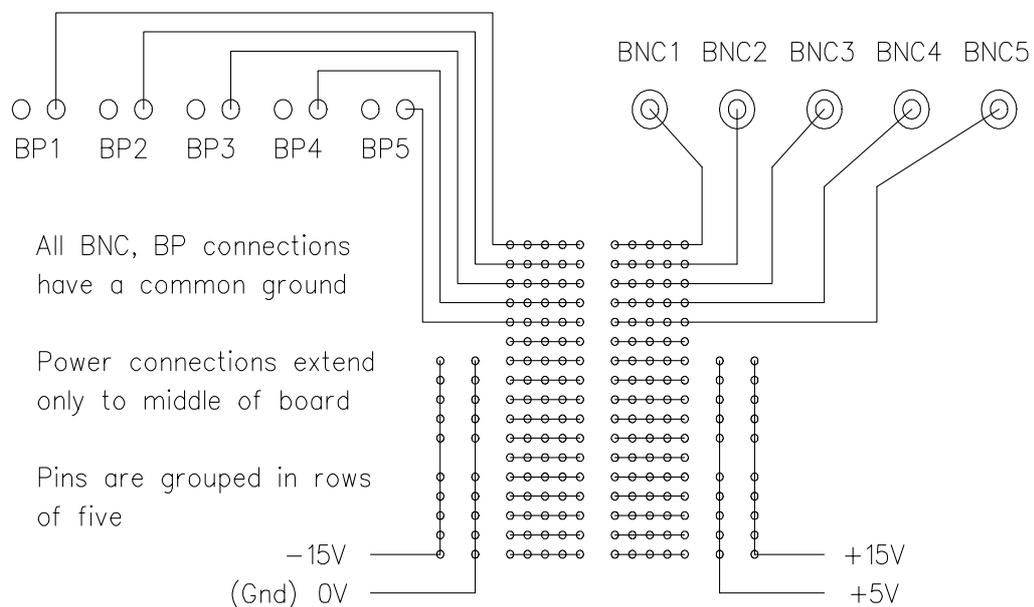


Figure 2.1: Electronics lab breadboard connection matrix

To make the experience of assembling a working circuit more enjoyable:

1. Be sure that the power is OFF;
2. verify by direct measurement the values of all the circuit components;
3. minimize the use of jumper wires by connecting components directly to one another;
4. verify that the jumper wires used are not broken (test for $0\ \Omega$ resistance);
5. assemble the circuit in a systematic and organized fashion;
6. check off each component as you add it to your circuit;
7. verify that your assembled circuit connections correspond to those of the schematic diagram.

Having taken the previous steps, turn ON the power and test the circuit for proper operation.

If the circuit does not behave as expected, you will need to do some troubleshooting. Use the schematic diagram as a guide to determine the voltage levels that should be present at various points of the circuit, then use a voltmeter to measure these nodes.

Develop a systematic approach to assembly and verification of the circuit that you are building. As the circuits get more complicated, you will find it advantageous to construct the circuit in stages, verifying the proper operation of the circuit after each progressive step.

2.2 Combinations of NAND gates implement other operations

Additional components required

- two 7400 IC chips and one 7473 IC chip
- four LEDs and five $470\ \Omega$ current-limiting resistors

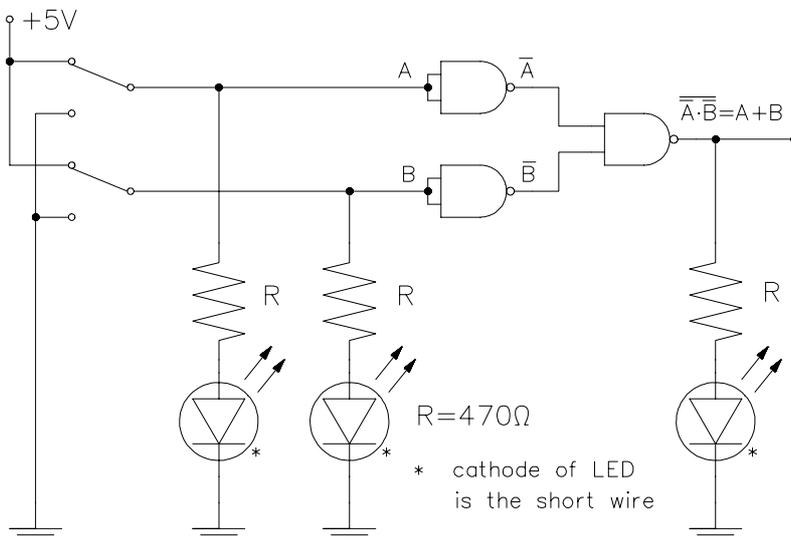


Figure 2.2: An OR gate made from NAND gates

NAND gates can be combined to form other logic gates. You must prepare for this lab by designing and drawing the schematic diagrams of the following circuits, made up entirely of NAND gates:

- an AND gate
- an exclusive OR (XOR) gate
- a half-adder
- a gated latch

In the example shown in Figure 2.2 three NAND gates form an OR gate. The LEDs on this diagram monitor the state of the inputs and the output. Each one is connected in series with a current-limiting resistor R .

Most integrated circuit (IC) chips contain a number of logic gates. In this experiment, the 7400 chip used contains four separate NAND gates. Make sure you start by making the power connections (ground and +5 V).

For each of the above circuits (an AND gate, an XOR gate, a half adder, a gated latch):

- ❗ Draw the circuit or create it using EWB. Label your gate connections with the corresponding chip gate pin numbers, as shown in Figure 2.4. This will ease the process of circuit assembly and troubleshooting.
- ❗ Assemble the circuit. Begin by installing the 7400 chip. Connect the power pins. Connect the gates and switches with jumper wires. Add the LEDs. Verify the correct orientation of each LED by connecting one end of the current-limiting resistor to the LED anode and the other end to +5 V. If the LED glows, it is inserted correctly. Re-connect the resistors as shown.
- ❗ Verify the circuit operation by testing all input combinations. Record the results as a truth table. For reference, data sheets that describe the logic states and expected operation of all these chips are available on the Web. You can verify your results using Electronics Workbench.
- ❗ Include in your report the Boolean explanation as done in the OR example, Figure 2.2.

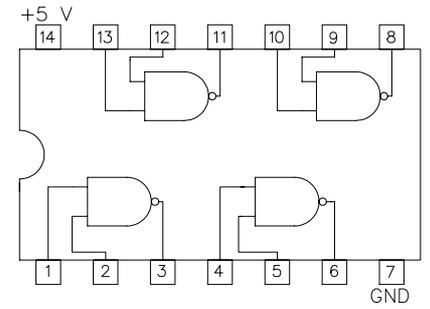


Figure 2.3: Pinout of a 7400

2.3 A binary counter

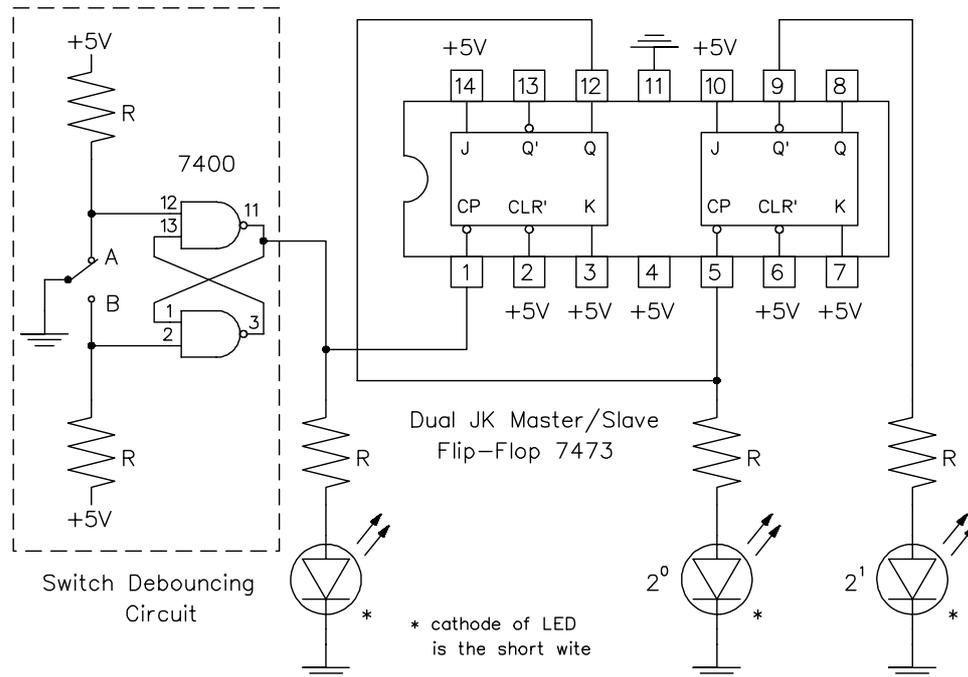


Figure 2.4: A binary counter

The binary counter, shown in Figure 2.4, is made using a 7473 dual JK flip-flop chip. This chip has several modes of operation, depending on the the signal levels at the J and K inputs. With

$J=K=+5$ V, the flip-flop performs a toggling function, so that the Q output changes logic state whenever a high to low transition occurs at the CP (clock pulse) input. Thus the Q output changes state at one half the rate of CP.

The switch, resistors and NAND gates make up a pulse generator that drives the counter input. When an electromechanical switch makes or breaks a contact, a series of pulses lasting some 1-5 ms are generated. This noise is known as *contact bounce* and is very undesirable in fast digital circuits. Since the gate delay and hence response time of flip-flops is around 10 ns, many pulses would be counted every time a switch is toggled, resulting in an erratic count. To *debounce* the switch, two NAND gates connected as an RS latch are used.

- ❓ Apply the above information along with the truth table for the RS latch to describe how the circuit debouncing is performed. Again, the Web or your textbook may be a useful resource.
- ❗ Assemble the switch, resistors, gates and LED for the debounce circuit, following the assembly procedures previously outlined. Document how the output of the debounce circuit behaves as the switch is toggled. Is this the behaviour of an RS latch?
- ❗ Add the counter circuit components. Graph the input pulses at CP from the debounce circuit and the values of 2^0 and 2^1 below one another and using the same arbitrary time scale. Switch movement $B \rightarrow A \rightarrow B$ represents a single input pulse.
Advise the demonstrator when the counter is working and demonstrate its operation.
- ❗ Remove the debounce circuit from the CP input of the counter. Reconnect the switch as follows: A to +5V, B to 0V, and the common point to CP. Toggle the switch. Graph the output states of the counter as you did before. Describe your results.
- ❗ Remove the switch from the CP input. Connect CP to one of the BNC1 contacts on the breadboard. Connect a cable from the BNC1 connector to the SYNC output of the signal generator. This output is a 0-5V square wave that can be used to clock digital circuits. Set the function generator frequency to 1Hz and describe the circuit behaviour.
- ❗ Slowly increase the frequency and note when each of the three LEDs changes from a noticeable on/off flickering to a steady glow. Estimate from these results, the response time of your eyes.

Lab Report

Submit a lab report consisting of the work undertaken during this lab. Start the report with an overall statement of purpose of the experiments. Then for *each* exercise include a sketch or printout of the circuit and graphs of the waveforms observed, formula derivations, a description of the theoretical behaviour of the circuit and comparison with your actual observations, and answers to the pertinent questions. The presentation of your results should be organized and complete, your diagrams titled and referenced, so that someone who is not familiar with the experiments would have no difficulty understanding what was done.

At the end of the lab report, include a brief Conclusions section that summarizes and compares the results from the simulated and hands-on portions of the lab and a discussion of any problems encountered and insights gained.