NAME (PRINT) | STUDENT ID | LAB DATE | GRADE

Experiment 3

Combinatorial and sequential logic

In combinatorial digital logic circuits the state of the outputs is determined by the state of the inputs, and a Boolean logic equation or a truth table can describe the function of the circuit in a very compact way. In the sequential logic, the state of the inputs at some earlier time may also matter, and a full desription of the function of the circuit involves a timing diagram, with logic levels, transitions between levels, and their time relationship presented together. Many circuits combine both elements.

All digital circuits require some time for an output to respond to a change of state at the input. This is known as the propagation delay of the circuit. This delay needs to be taken into account in order to to properly analyze circuit behaviour and timing.

3.1 Divide-by-two flip-flop

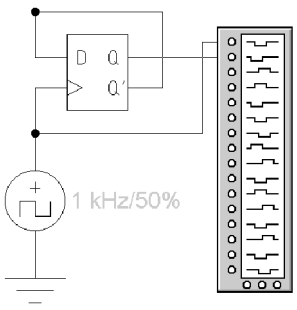

Figure 3.1: A :2 flip-flop

A D flip-flop propagates the state of its input D to the outputs Q and $\bar{Q}$ at the rising edge of the clock pulse, CP. The output is held after CP goes low. In the "feedback" mode, where $\bar{Q}$ is connected back to D as shown, it will take two clock cycles to return to the initial state. Thus a single D flip-flop performs a simple divide-by-two.

(!) Assemble the circuit shown. Use the logic analyzer to monitor the timing of the divide-by-two operation. The logic analyzer samples the logic states of the input lines at a rate determined by an internal or external clock. Check by double-clicking on the analyzer icon that this internal clock is selected and set to a frequency of 5-10 times that of the input signals, otherwise you may not see any meaningful analyzer output.

(!) Add the extra connection between the $\bar{Q}$ and the logic analyzer to monitor the second output as well. Make a record of the analyzer timing diagram.

(!) Increase CP and the analyzer clock to observe and determine the *propagation delay* from CP to the Q outputs. Record the analyzer output.

[?] Consider the relationship between the various signals in the two timimg diagrams. Why does the timing in the two diagrams seem to differ? Based on your observations, write down the

truth table for a D flip-flop. Compare with that of a real D flip-flop device, such as a 4013, by reviewing the device data sheet.

3.2 A binary counter with D flip-flops

Several D flip-flops connected in a chain perform as a binary ripple counter, each stage undergoing a change of state half as frequently as the previous one. In this circuit, slow the clock down to 1 Hz or so, and use just a set of LED indicators to read off the binary count.

(!) Assemble the circuit as shown and verify its operation. You may want to assemble one binary digit first, then select several circuit elements, and Copy and Paste several times to expand to more digits. Label the most- and the least-significant bits as MSB and LSB, respectively.

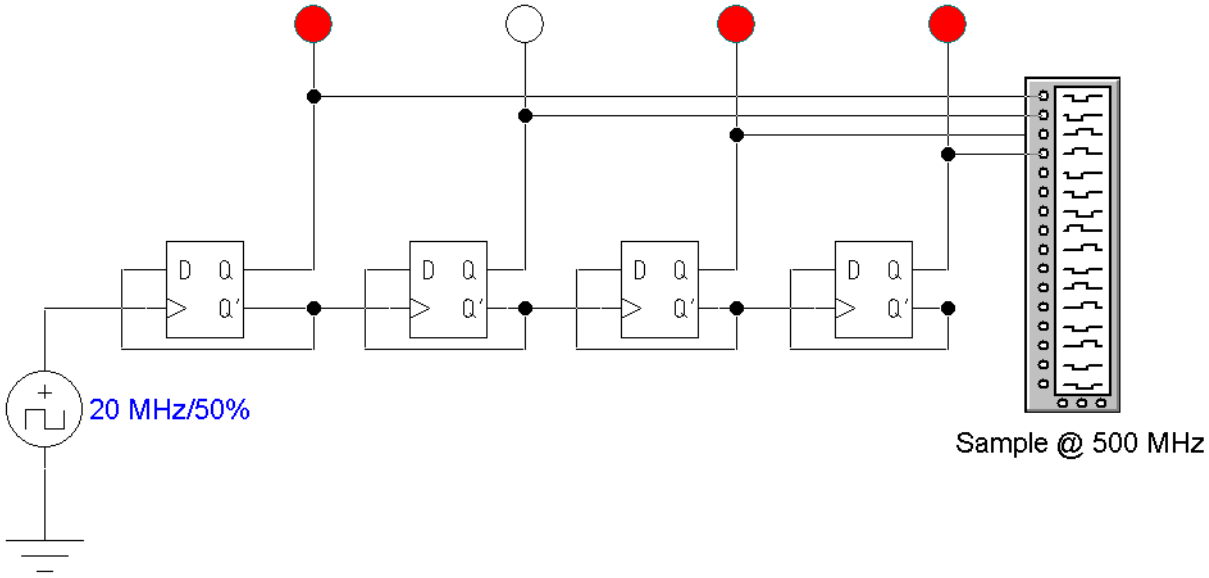

Figure 3.2: A binary counter

[?] The logic analyzer allows you to monitor the output waveforms and thus to verify the operation of the counter. Taken together, the four Q output lines represent a 4-bit binary value; how does this value change with every transition of the clock? How does the value at the Q' outputs change? Explain.

[?] Determine the propagation delay for each of the flip/flops and then the total propagation delay of the entire ripple counter of Fig.3.2. What is the maximum clock rate that should be applied to this circuit? How do the outputs behave as the circuit is *overclocked* beyond this maximum frequency? Explain this behaviour in terms of propagation delays.

[?] Predict the propagation delay of a 10-bit ripple counter. iHow does the propagation delay affect the size of a ripple counter? Is this a desirable characteristic in a counting circuit?

3.3 One-of-eight decoder

A key device needed in multiplexing/demultiplexing applications is a binary to one-of-eight decoder, similar to the one shown in Figure 3.3.

(!) Assemble the decoder as shown, drive it with the binary counter from the previous section, and verify that only one of the lights at a time, in sequence, are turned on by the binary counter.

[?] Use the analyzer to record the complete timing diagram for the 3-bit binary to one-of-eight decoder, including the clock pulse waveform.

[?] Given that all digital components in EWB exhibit by default a 10 ns propagation delay, what is the propagation delay from the clock to each of the decoder outputs? Verify this by observing the analyzer output. How could you decrease the propagation delay of the counter/decoder circuit in Figure 3.3?

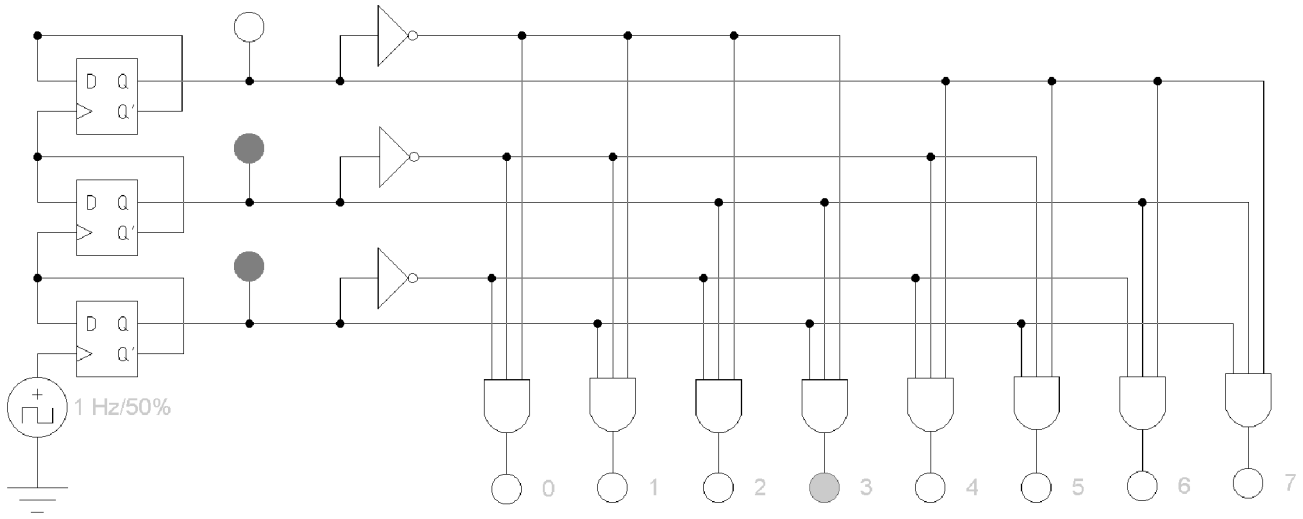

Figure 3.3: Binary to one-of-eight decoder

3.4 A design challenge

The challenge is to design an extension of the decoder circuit that lights a green indicator if and only if a special sequence (a password) of two 3-bit numbers is presented at the input, and a red indicator for any other combination of two input numbers.

(!) Sketch a flowchart of the logical steps that are required to solve the problem. From this, develop a timing diagram of the different signals that your circuit needs to generate.

(!) Replace the binary counter with the pattern generator. Verify that you know the pattern of 3-bit inputs that turns on any desired light. Note that the *Data Ready* output of the pattern generator makes a low-to-high transition when the the next data word is latched at the outputs.

? Monitor the circuit with the logic analyzer. How does the timing of your circuit compare with that of your timing diagram?

? How would you expand your circuit to decode a series of three 3-bit numbers?